# X2000 Power System Electronics Development

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*Abstract*—The Deep Space System Technology (DSST) Program (X2000) is managed by JPL for NASA. The program will provide advanced flight and ground systems for the exploration of the outer planets. The X2000 Integrated First Delivery Project under DSST is to provide flight avionics for the first set of mission customers—Europa Orbiter, Pluto/Kuiper Express, and Solar Probe.

These missions provide a challenge in terms of extreme environmental requirements. The key driving requirements are the one-mega-rad total ionizing dose and the 15-year life span.

The X2000 Power System Electronics (PSE) must reduce its power, mass and volume envelope by incorporating new technologies developed by industry partners. The combination of multi-chip module (MCM) packaging, radiation-hardened (rad-hard) mixed-signal application-specific integrated circuits (ASIC) and next-generation power devices increases the packaging density of the PSEs.

The PSE modules combine high-density packaging techniques and mixed-signal ASICs for a reduction in mass and volume without sacrificing functionality or efficiency.

## TABLE OF CONTENTS



## 1. INTRODUCTION

*Deep Space Systems Technology Program*

The X2000, managed by JPL for NASA, has taken the prime initiative to develop new technologies that enable deep space missions. The X2000 Program is composed of several elements. Following is a relevant subset of the elements pertaining to this paper:

- X2000 Integrated First Delivery Project (X2000 IFDP)
- Advanced Radioisotope Power Source (ARPS)
- Center for Integrated Space Microsystems (CISM)
- Mission Data System (MDS)
- Future Deliveries (D2+)

The thrust of the program is to deliver a series of spacecraft avionics packages that will meet the requirements of upcoming outer planet missions. Each element is to provide dramatic technology breakthroughs enabling higher levels of integration.

The primary focus of the X2000 IFDP element is on the delivery of a flight avionics package for the Outer Planets and Solar Probe (OPSP) Program. The package will include a new and innovative distributed architecture in both hardware and software. The architecture must be capable of integrating different instruments, propulsion modules, power sources, and telecommunication into a multiple mission platform.

The ARPS element will develop a more efficient ~~and robust~~ advanced radioisotope power source that will meet the requirements of future outer planet missions.

The CISM is a center of excellence focused on higher levels of integration for spacecraft avionics. CISM will develop new technologies that enable higher levels of integration with the foresight of future systems on a chip.

The MDS element will provide a flight and ground data system that will be used for several deliveries. MDS embodies the end-to-end system architecture. The X2000 IFDP will deliver an integrated avionics package for the first delivery.

The D2+ element focuses on the needs of the customers beyond the first delivery. A considerable amount of the first delivery will be leveraged and enhanced for future deliveries.

The ~~OPSP program~~ OPSP project is the first customer to use the X2000 IFDP Avionics. The program includes the following missions planned for launch within the next decade:

- Europa Orbiter (EO) ~~(Launch 11/03)~~
- Pluto Kuiper Express (PKE) ~~(Launch 11/04)~~
- Solar Probe (SP) ~~(Launch 8/07)~~

Each mission offers difficult challenges that are reflected in the following key requirements:

- One mega-rad total ionizing dose(EO)
- Fifteen-year life (PKE)
- Low mass and power (EO)

With all of the challenges in the first set of missions, a combination of new technology and innovative architecture is needed.

## 2. Development Approach

The PSE approach to meeting the needs of the customer is to combine a new architecture with the development of new technology. The program has limited funding, making the overall cost a key development driver.

Based on JPL's experience in developing the Cassini power system, the combination of rad-hard ASICs and high density packaging can be implemented to increase overall functionality, reduce mass, and lower both development and recurring cost.

The Cassini Power System uses a Solid State Power Switch (SSPS), which is combined with a rad-hard digital ASIC with discrete analog and power components in a class-K hybrid package (figure 1). The SSPS was produced by CTS Microeletronics under contract from JPL.

The Cassini SSPS hybrid contained the following components:

- 2 UTMC gate arrays
- 35 active devices (IC dice)
- 26 chip resistors and capacitors
- 181 screened resistors
- 12 actively trimmed resistors
- 466 bond wires (396 are 1 mil gold)
- 72 pin package

Cassini also utilized a Honeywell (HR1060) one-mega-rad-hard gate array for the power distribution command

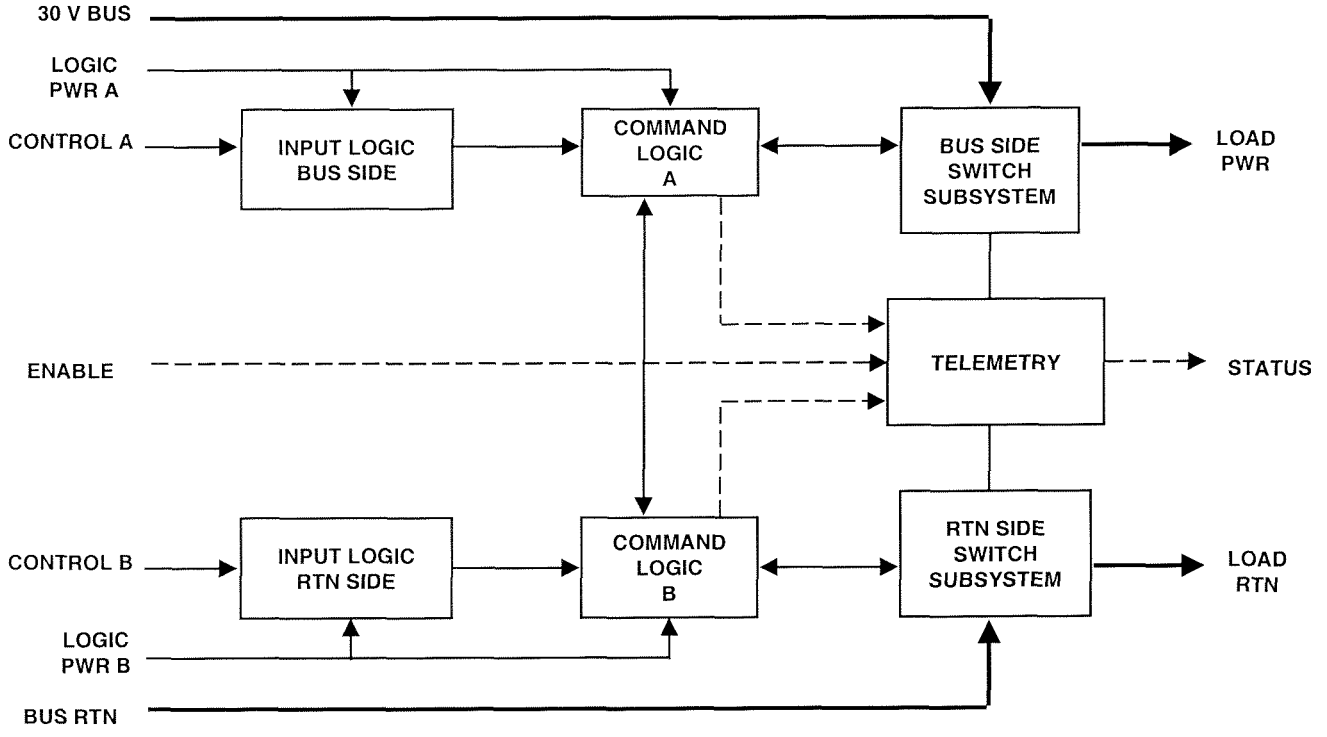


**Figure 1** Cassini SSPS

interface. The power distribution contained a custom serial data bus on every board. The main command interface from the spacecraft was through a remote engineering unit (REU) providing a 1553 data bus to the spacecraft and a parallel interface to the power subsystem.

This development paid off for Cassini because the components were used on every power distribution board. The use of custom components on every board reduced the number of piece parts and assembly time for each board. Cassini was able to provide more functionality in a smaller package by investing in hybrids and gate arrays.

In a similar approach, the X2000 PSE would like to go one step beyond Cassini and implement mixed-signal ASICs and MCMs.

Cassini was successful in using existing technology to provide modules. However, with today's technology, there is room for improvement. With the use of mixed-signal ASICs, the number of components can be reduced even further than what was accomplished on Cassini.

Other improvements over Cassini can be accomplished through the selection of a mixed-signal ASIC technology. By selecting a technology that is compatible with the command and data handling (C&DH) ASICs, the power system can use the same Intellectual Property (IP) for C&DH and the mixed-signal ASICs in the power subsystem. This will provide a standard interface to each of the power system boards that is well supported by the overall system.

*Power System Goals*

Following is a list of goals for the X2000 PSE that relates directly to the goals of the X2000 Program:

- Multiple-mission architecture
- Increased power management
- High end-to-end system efficiency

To meet the goal of a multiple-mission architecture, the PSEs must be a modular, scaleable design with standard interfaces.

The architecture of the power system needs to be partitioned in modules that can be interchanged depending on the mission requirements. Partitioning the design, so that only a single module is affected by a different source, energy storage technology, or unique load, can reduce the cost of a multiple mission platform.

The power system architecture developed must utilize this modular philosophy without sacrificing the capability for design optimization. This requires a combination of MCM packaging with accessible surface mount packaging. With intelligent partitioning of the power system functions, a modular design can evolve with the capability for late changes and minor optimization.

Functions that are common throughout the power system, such as power switching, pulse width modulation, and the command interface, can be incorporated in mixed-signal ASICs or MCMs with little concern for future modification. These functions are considered the core building blocks for the power system.

Another goal of the power system is to provide more power management capability, which will enable missions with very low power source capability. Power is a limited resource particularly for outer planet missions where generating power becomes more elusive.

More system visibility in the form of telemetry and power switching enables the system to improve its management capability. By increasing the number of power switches and telemetry channels, the system has more options for accomplishing the mission requirements within the allocated power.

Improving the overall end-to-end system efficiency is a long-standing power system goal. Multiple types of power converters in the system provide more system development risks, when it comes to overall efficiency and system stability. Many of the different types of converters are underutilized and thus operate at the lower end of the efficiency curve.

The development of a power converter that meets the system-input-impedance and conducted-emissions requirements, and provides high efficiency over a wide load range can reduce risk and improve efficiency. A generic converter offering the most common output voltages can be developed using the latest technology. This converter could be offered to the users to allow them to take advantage of the latest technology without the risk.

The users would have to be willing to settle for a generic capability power converter, but the payoff to the power system could be great. The power system would be dealing with many of the same converters known to meet the input impedance and conducted emissions requirements. For this to be effective, the converter needs a high efficiency over a wide load range and must come in a small package to make it attractive to the end user.

To be successful, X2000 will have to focus the non-recurring engineering (NRE) on only a few functional building blocks. The architecture needs to leverage the building block approach and reduce the number of point designs to reduce the overall cost of the program.

*X2000 PSE Objectives*

The primary objectives for the X2000 IFDP PSEs are:

- Develop a one-mega-rad-hard analog cell library
- Produce several mixed-signal ASICs

- Fabricate a select number of power MCMs
- Deliver PSEs Boards

It is clear from the objectives that delivering a power subsystem is not enough. The X2000 charter will pave the way for future developments over several deliveries. More than a hardware delivery, the objectives reflect a methodology for the follow-on deliveries to use.

The development of a one-mega-rad-hard analog cell library provides a consistent path for future deliveries to use as a tool in developing ASICs. A good library can be used for the specification of different ASICs that is independent of the foundry. The library can be maintained separately and targeted to different foundries as technology improves. This allows for the new foundries to be qualified with the library before the first specific ASIC design needs to be fabricated. Specific ASIC design can be passed from one delivery to the next with only a higher-level chip layout and simulation required.

The development of mixed-signal ASICs for applications repeated throughout the power subsystem can provide consistency in performance over the environmental requirements. The performance of these functions can be proven and repeated, reducing the number of piece parts in the system and lowering the risk in system integration. These ASICs are designed using the same analog cells and also share larger macro cells. The ASICs make it possible to meet the X2000 environmental requirements.

Just as mixed-signal ASICs are used, high density MCMs can also be used to provide functional building blocks for the power subsystem. The MCM packaging approach enables the close packaging between the discrete power components and the ASICs. These power MCMs will provide complex power circuits in a dense modular package. Most of the difficult design, layout, and analyses will be completed at the MCM level, thus reducing the complexity on the circuit board.
The finished product will be power subsystem circuit boards that can be configured into a mission-specific power system. The purpose of the circuit boards is to bridge the gap between the power electronics building blocks and the mission specific subsystem. By investing NRE in the MCMs, the circuit boards can be easily modified with little NRE to match the packaging concept of any mission. The circuit boards are a higher-level building block that can be configured to meet the mission needs.

All of the objectives are considered deliveries to the X2000 program. These objectives are in place to build a foundation for power system development with the long-term goal of system on a chip.

## 3. KEY TECHNOLOGIES

Technology development has been very limited for many projects. The high NRE costs and schedule needed for technology development limit what many projects achieve. Additionally, the associated risk prevents many project managers from investing in new technology.

Fortunately, with the formation of CISM for technology development and the New Millennium Program (NMP) for flight validation, new projects can benefit with reduced risk, while industry can demonstrate promising new technology.

The goal of CISM and the NMP Microelectronics Integrated Product Development Team (IPDT) is to develop and validate promising new technologies, modular building block designs, and standard interfaces. The IPDT has a number of members from industry, universities, laboratories, and NASA with a common goal of producing a road map of technology needed for the next generation of spacecraft.

JPL is partnering with key industry leaders to focus the technology development and provide an application for its use. The industry partners are Boeing Solid State Electronics Center (SSEC) and Lockheed Martin Communication and Power Center (LM-CPC). This partnership has worked well in developing the power actuation and switching module (PASM, see figure 3) for the Deep Space One (DS1) mission in the New Millennium Program.

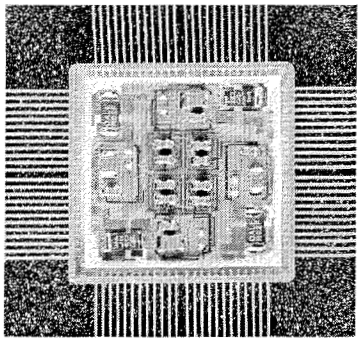

**Figure 2** DS1 PASM

The goal of the PASM experiment is to flight validate two promising technologies for the PSEs. The technologies are the high-voltage mixed-signal ASIC and the power high-density interconnect (PHDI) packaging.

The PASM has four power switches that are current controlled for soft start, with current limiting and tripping functions. It provides the same functionality as the SSPS in a much smaller package. The PHDI switch module was designed by LM-CPC utilizing General Electric (GE) technology. The PHDI packaging technology combines the mixed-signal ASIC, power MOSFET, and discrete components of four switches in a single package. The PHDI packaging technology enables high-density packaging for power applications.

Boeing designed the switch control ASIC (SCA) that provides the control functions for the power switch. The SCA was fabricated on the Harris Radiation-Hardened SiGate (RSG) process. The SCA combined the functionality of the SSPS gate array and discrete analog components into a single component.

Other technologies have also been considered for use in the X2000 program. Boeing designed the Power Management ASIC and Advanced Instrument Controller for the NMP Deep Space 2 probe. LM-CPC developed the all PHDI Electronic Power Converter (figure 3).

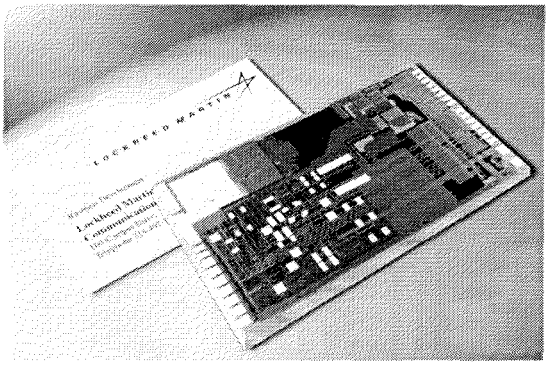

**Figure 3** LM-CPC EPC

All of these technologies were leveraged in some way in the X2000 PSE development.

## 4. POWER SYSTEM ARCHITECTURE

The X2000 PSE architecture (figure 4) is conceived to meet the goals of X2000. It is scalable and expandable for different mission power levels and redundancy requirements. It provides a high level of insight into the status of the power system and individual loads, and it uses the highest efficiency components available.

The X2000 IFDP power system is a direct energy transfer or battery-dominated bus. Alternate architectures can be achieved with the addition of a few more building blocks. These additional building blocks are not within the scope of the IFDP. The PSE slices can be used in alternate architectures if desired by the missions.

The power system architecture consists of unique functional slices that can be optimized for a specific power source, energy storage technology, or load requirement. These slices are connected together via the power bus and the I2C data bus. Each slice has the same power and data interface. The standard interface allows for missions to add slices as needed based on the power level and number of loads. The slices are configured by the backplane.

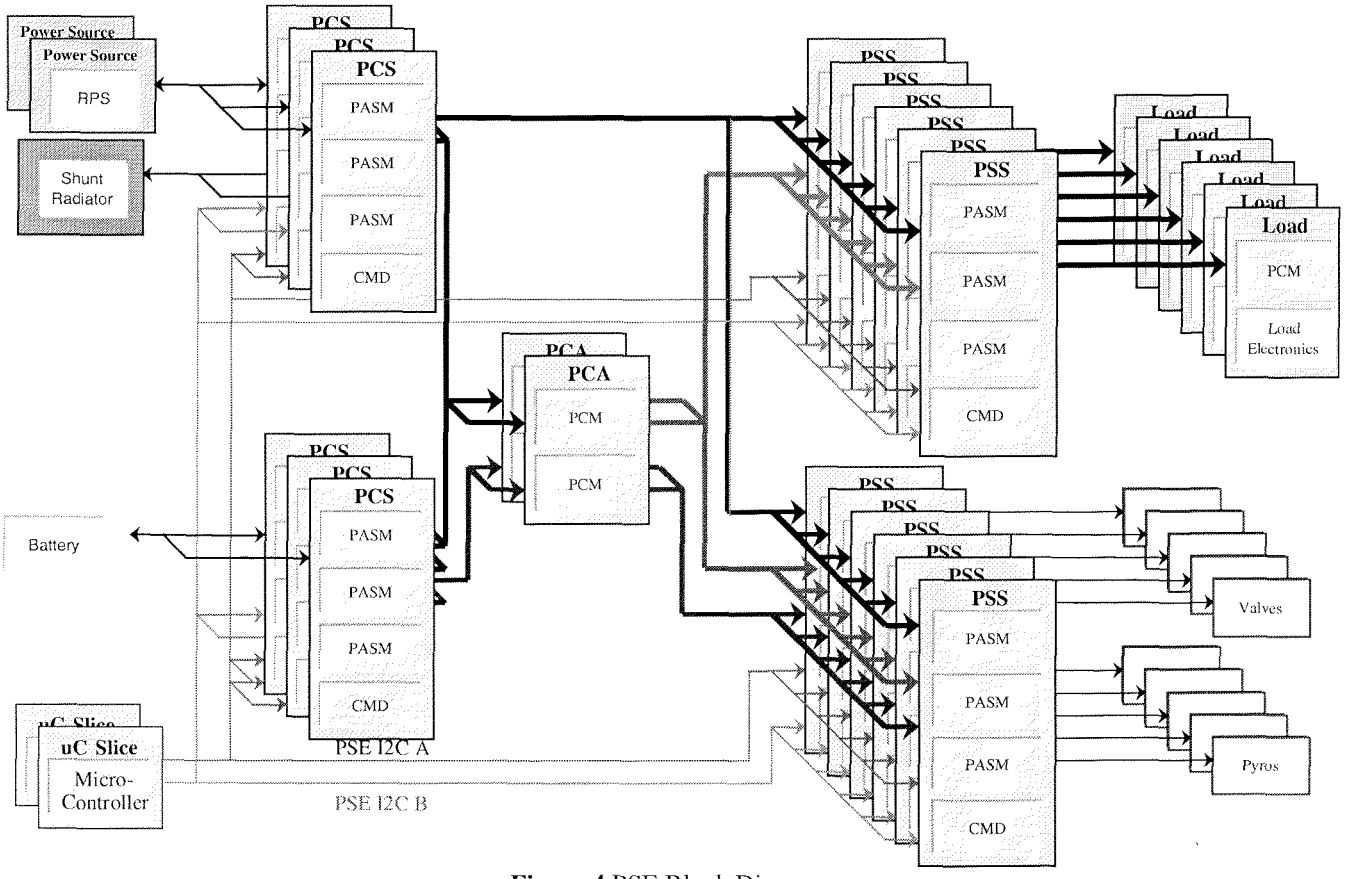


**Figure 4** PSE Block Diagram

The packaging approach for the PSE is to use the Compact peripheral component interconnect (PCI) standard 3U card cage (figure 5). All the PSE slices will be double-sided 3U cards with an average mass of 500 g.

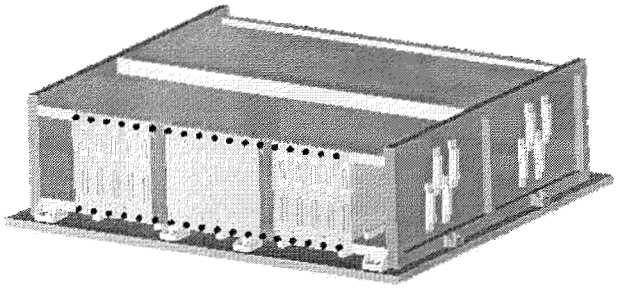

**Figure 5** PSE Chassis

The cards will plug into a backplane that can be used to distribute the power bus and set the configuration of the circuit boards.

There are three types of slices:

- Power control slice (PCS)
- Power converter assembly (PCA)
- Power switch slice (PSS)

Each slice will use the power electronic building blocks. There are two power electronics MCMs:

- Power actuation and switching module (PASM)
- Power converter module (PCM)

Each MCM contains mixed-signal ASICs and discrete power components. Another functional building block is the command interface ASIC (CIA). The CIA is a mixed-signal ASIC with some discrete component on the circuit board. The following paragraphs are brief descriptions of the functionality of each slice. For a detailed description of each slice, refer to the Section 5.

The PCS provides the main interface with the power source. The primary function is to regulate the power bus voltage and/or battery charge current. It achieves regulation by digitally switching bus shunt loads to control the bus voltage or battery current. The PCS will have programmable set points for both the bus voltage and battery charge current. Power control also provides all of the fault protection and telemetry for the power bus and battery. Single fault tolerance is obtained by majority voting three slices to provide that control function. The CIA provides the command and telemetry interface and control algorithms. The PASM provides the power switching.

The PCS, configured differently, also provides the main interface to the battery. The main function is to provide a battery cell bypass to prevent overcharging of the cell. The bypass cell voltage set point is programmable. Single-fault tolerance is obtained by voting three slices. The CIA provides the command and telemetry interface and control algorithms, and the PASM provides the power switching.

The PSS provides the interface to all of the loads on the spacecraft. Each power switch can be commanded to drive a steady state or momentary/pulse load. Each switch can be configured in the high or low side, and series or parallel. No single failure shall cause more than one switch to be stuck ON. Telemetry is provided for each load. Every switch in the PASM provides controlled turn on and protects the power bus from load faults. The CIA provides the command and telemetry interface. The PASM provides the power switching.

The PSS also provides the power and command interface to the valves on the spacecraft. The CIA can synchronize and provide accurate timed commands. The same protection and telemetry is also provided per valve interface.

Finally, the PSS provides the interface to the pyro devices. The PSS provides an interface for safety inhibits, and has separate enable commands for groups of switches. Each switch provides current limiting to allow for simultaneous multiple events.

The PCA provides the house-keeping power for the power system. Each slice requires a redundant 3.3V and 5.0V housekeeping power. The 3.3 V is for the digital logic, and the 5.0 V is for the analog control functions. Power-cross-strapping is done internally on each slice. The PCA just contains one 3.3 V PCM and one 5.0 V PCM.

Each power system slice has the same standard I2C data bus interface, which enables the spacecraft computer direct access to each module. This results in test and integration cost decreases due to having an industry standard interface combined with increased visibility into each module during system-level testing.

The purpose of this architecture is to give missions more flexibility to configure a power system that meets their requirements. The architecture provides all of the hooks needed for a robust configuration. The ultimate reliability of the subsystem depends greatly on the configuration of the slices. The architecture provides many options for redundancy and can be scaled based on the mission requirements. The PSEs can be configured as a single string or 1 thru N redundancy.

## 5. PRODUCT DESCRIPTION

The following subsections will elaborate in more detail on the X2000 PSE products.

*Rad-Hard Analog Cell Library*

Much of the PSE is based on the functionality provided in the analog cell library. The purpose of the library is to allow qualification of the cells to occur prior to the development of the ASIC.

The complexity of the cells ranges from simple operational amplifiers and comparators to more complex macro cells such as an auto-zero amplifier or pulse width modulator. These cells make up the lowest level of building blocks for PSEs.

The foundry selected for the library is the Honeywell RiCMOS IV process. Honeywell has shown that they can achieve one-mega-rad-hard performance on this line. Other advantages to the line are that it is a proven digital process with a large library of digital cells and IP.

Boeing is the industry partner developing this library. Many of the cells have been fabricated and tested verifying the post radiation models.

Boeing has provided an innovative high-voltage transistor on this low-voltage process based on the work performed by Professor Mohammad Mojarradi of Washington State University. This development has been a key to enabling power control functions to be done on a low-voltage mixed-signal process.

*Rad-Hard Mixed-Signal ASICs*

The following rad-hard, mixed-signal ASICs are being developed:

- Pulse Width Modulator ASIC (PWMA)
- Synchronous Rectifier Controller ASIC (SRCA)
- Switch Control ASIC (SCA)
- Command Interface ASIC (CIA)

Each ASIC is based on the analog cell library and digital macro cells provided by C&DH.

The PWMA and SRCA are used in the power converter module. The PWMA is on the primary side of the isolated converter and provides the pulse width modulation and synchronous rectification driver functions. The SRCA is on the secondary side of the converter and provides the synchronous rectifier drivers.

The SCA is the most used part in the PSE with an estimated quantity of over one thousand for first delivery. This is a perfect example of when an ASIC can be economical. The SCA provides all of the control functions for each switch in the PASM. The SCA also provides the level shifting and charge pump for high-side power switching.

The CIA provides the system interface for all of the boards. The CIA is comprised of an integrated 8051 core, memory, analog to digital converter (ADC) and a Philips I2C data bus interface. The CIA provides a single chip solution to the command interface that was handled by the REU on Cassini.

*Power Converter Module*

The X2000 PCM design (figure 6) is a DC/DC converter that operates at high frequency (1 MHz) providing high efficiency and small volume (2.0" × 3.0" × 0.4").

The PCM provides an output power level of 30 W (figure 7), and output voltages of 3.3 or 5.0 V. The input bus voltage is specified from 22 to 36 $V_{DC}$. The converter provides output overvoltage and load short-circuit protection by latching off the converter.

The converter is designed to meet conducted and radiated susceptibility electromagnetic compatibility (EMC) requirements, including input power line transients. Isolation requirements are one mega-ohm at +/- 30 $V_{DC}$, primary to secondary.

The topology is a dual resonant forward converter operated at a fixed switching frequency. Output voltage regulation is achieved by pre-regulating the dual-forward-converter primary voltage with a hard switched, pulse-width modulated buck converter. The resonant forward converter stages provide high efficiency by virtue of their zero voltage switching characteristics. The converters operate at 180 degrees out of phase to minimize input and output filtering. Output rectification losses in the high current low output voltage designs, are reduced by utilizing synchronous rectifiers. The resonant forward converter section is easily optimized because the input voltage is pre-regulated.

Efficiency is maximized by the use of a complementary hetero-junction field effect transistor (CHFET), developed by GE and Honeywell. The CHFET has the advantage of having low- input capacitance and a low input drive voltage. Both of these parameters reduce the power necessary to switch at the 1-MHz switching frequency. In addition, the CHFET structure does not contain a parasitic Source/Drain body diode, which makes them ideal for a synchronous rectifier. There is no danger of a body diode conducting/avoiding reverse recovery issues.

*Power Actuation and Switching Module*

The second-generation PASM is very similar to the DS1 version. It provides basically the same funcitonality but with a one-mega-rad-hard rating. The PASM contains four independent solid state power switches in a single package. The following is a list of switch parameters for the PASM.

| | |
|---|---|
| Overload Trip Current | 1 A, 3 A (selectable) |
| Overload Trip Delay | 20 ms |
| Current Limit | 2 A, 5 A (selectable) |
| di/dt | 180 A/S |
| Voltage Telemetry | 0.075 V/V |
| Current Telemetry | 1 V/A |
| On resistance | 60 mOhms |
| Input Voltage Range | 0 – 40 V |

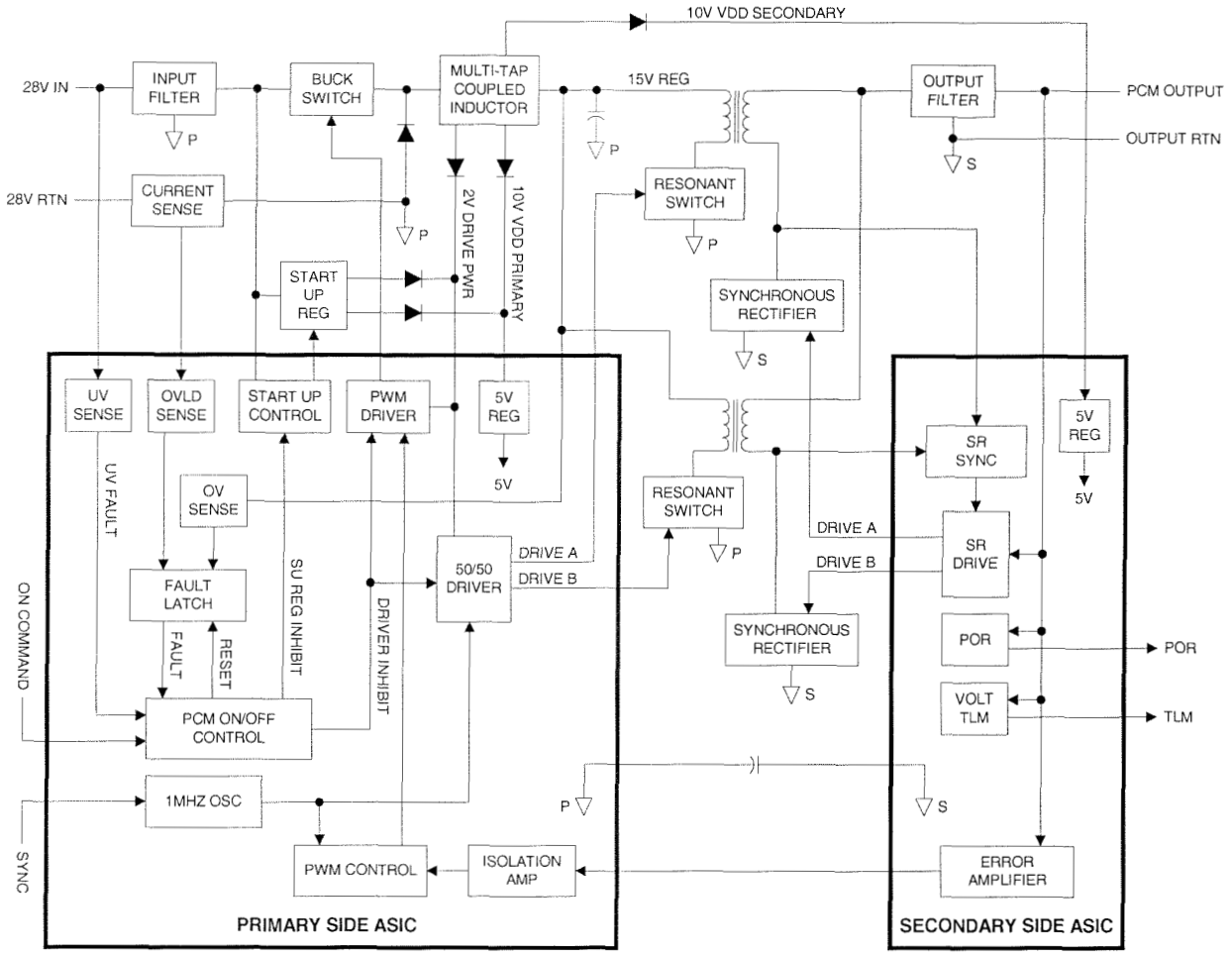


**Figure 6** PCM Block Diagram

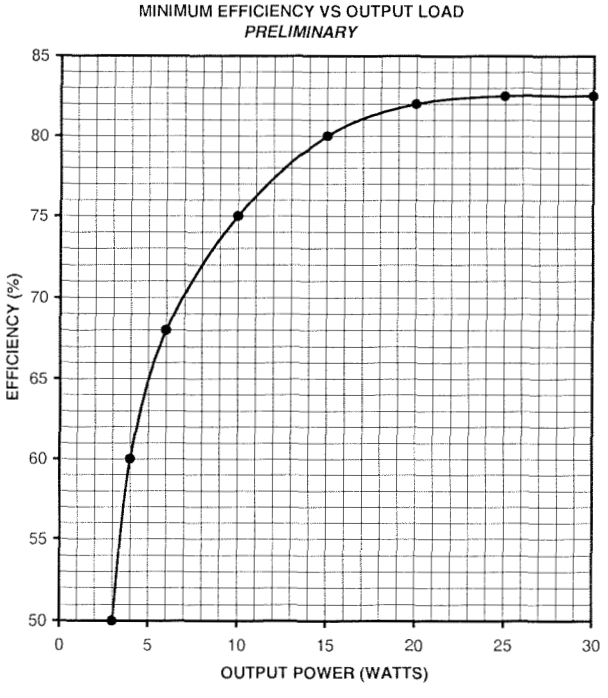


**Figure 7** PCM Efficiency Curve

Some changes have been made to make the PASM more compatible with the X2000 products. The SCA is on the Honeywell RiCMOS IV, therefore the PASM is now one-mega-rad hard. Another change is that the package has changed to fit three PASMs on a side within a Compact PCI 3U card.

*Power Control Slice*

The PCS is configured as a set of generic PASMs driven by an 8051 micro-controller control interface assembly (CIA). In this way, the PCS can be used for a variety of functions under the direction of local software. A functional block diagram of this concept is shown in figure 8.

The approach of using the CIA and the PASM for power control functions reduces overall NRE by avoiding specialized control ASICs. This is a case where functional building blocks can be used in other applications even when not optimized for it. Within the X2000 PCS the functions can be broken down into two categories: power control functions and battery control functions.

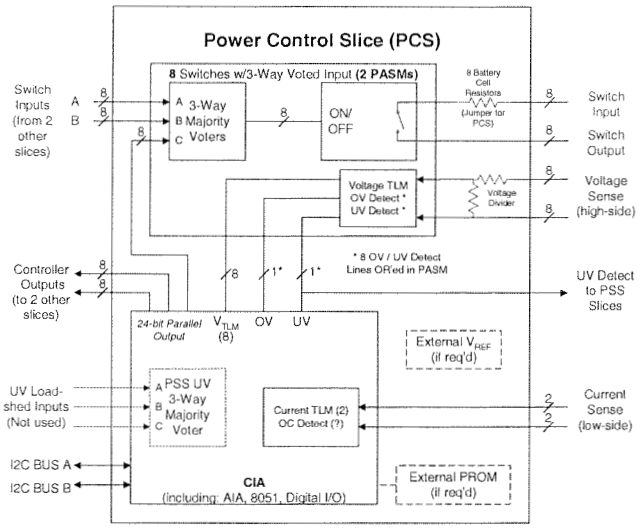


**Figure 8** PCS Functional Block Diagram

The fundamental power control and battery control software and default states/values will be contained in non-volatile memory. Software parameters or advanced management algorithms can be loaded into RAM. Due to a limited amount of ROM available within the CIA module, it may be necessary to include external ROM on the PCS slice.

*Power Control Function*

The power control function will use the PCS to switch in digital shunts to control the bus voltage and/or battery charge current.

The PCS monitors bus voltage and battery-charge current telemetry and compares them against a command value. PCS shunt switches are sequentially turned ON to divert RTG output current to ground, thus reducing the current onto the battery bus (and hence the bus voltage). PCS shunt switches are sequentially turned OFF to increase the RTG current onto the battery bus. The PCS control loop acts to balance the amount of RTG current available to the battery bus with the spacecraft load demand plus the desired battery charge current.

If the spacecraft load plus battery charge requirement equals the total RTG power, all PCS shunts will turn OFF. If the spacecraft load plus battery charge requirement exceeds the total RTG, power the battery charge current will naturally cut back toward zero. If the spacecraft load current alone exceeds the total RTG power, the battery will be discharged to supply the deficit. At this point, the battery/bus voltage will drop according to the battery voltage vs. state of charge (SOC) characteristic.

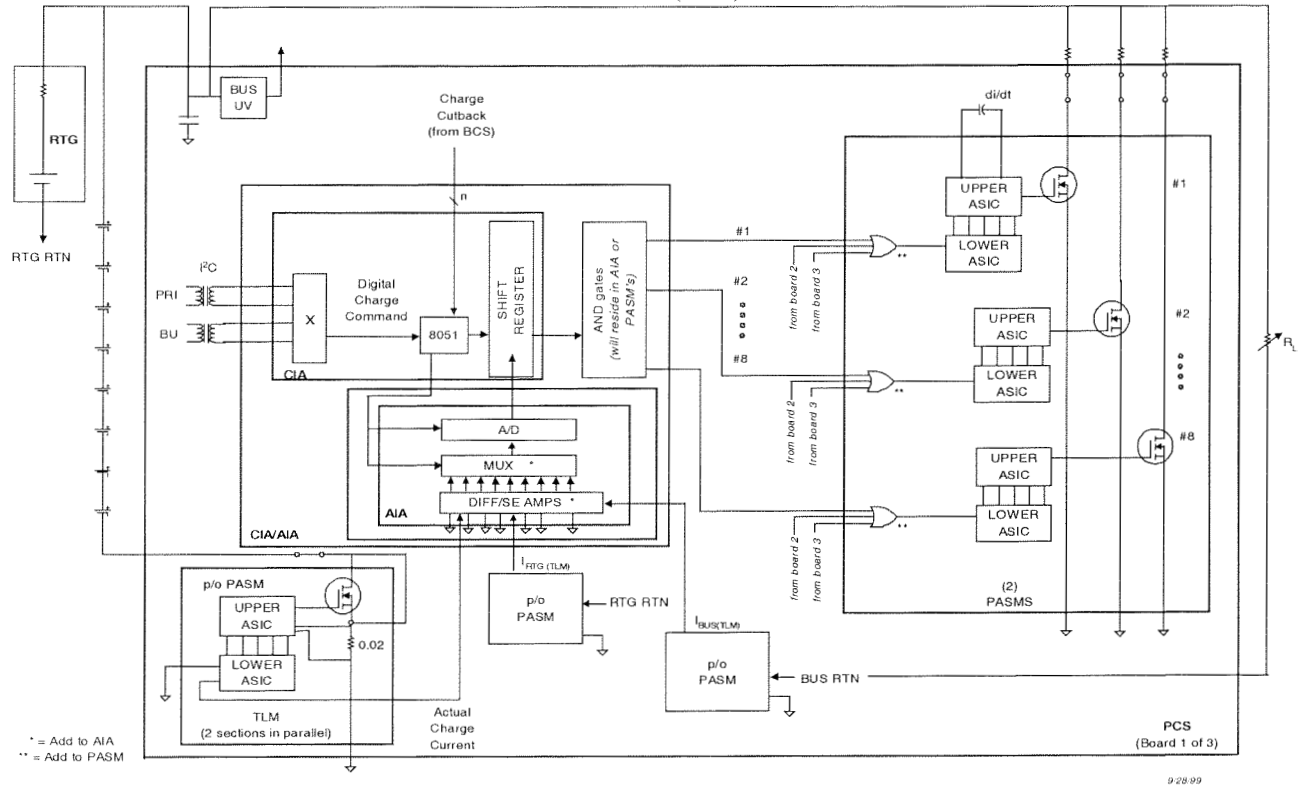


**Figure 9** PCS Block Diagram

**Table 1**: Power Control Parameters

| | | |
|---|---|---|
| Number of shunt load switches | 24 Total | 24 for 23 Redundancy |
| Total Shunt Power | 300 W | Equivalent to Maximum RTG source power |
| Power per Shunt Switch | 13 W | 300 W / 23 switches |
| Battery Charge Current | Maximum: 1C (6A)<br>Nominal: C/3 (2A)<br>Minimum: 0<br>Increment: < C/50 (0.12A) | Battery Driven Requirement TBC |

*Battery Control Function*

The battery control slice (BCS) system monitors eight (8) individual battery cell voltages. During re-charge, as any battery cell exceeds a programmed maximum voltage, the BCS switches a bank of 3 resistors across that cell to bleed off excess charge current.

Once a cell reaches the maximum voltage again (with all resistors across it), the BCS issues a "charge-current-cutback" signal to the PCS function to reduce the bulk charge current into the battery. This cut-back cycle will repeat in order to limit the cell voltage by "tapering" the charge current into the battery stack. Eventually, the charge current provided by the PCS function is reduced to a minimum value. This minimum value will be equal to the amount of current bypassed by all three (two in the case of a switch OFF failure) battery resistors ON at the programmed maximum cell voltage. The highest cell will remain with resistors switched ON such that the net charge current into this cell is zero.

Using this control scheme, the cell with the highest voltage will dominate the charge cut-back/tapering function, but it cannot reduce the bulk charge to zero. This gives the lower voltage cells a chance to "catch up" to the highest—albeit at a reduced charge rate. (In practice, the expected voltage divergence from cell to cell is low enough that the lower cells should not take too long to catch up.) The lower voltage cells will cycle their resistors in order to modulate their charge current until they have reached full charge. Then their resistors will remain on continuously. Thus, even when all cells are fully charged to their maximum voltage, a constant "trickle" charge will be flowing from the bus through the battery system. This continuous trickle mode of operation provides continuous cell-to-cell voltage balancing.

*Power Switch Slice*

Just as the PCS is used for multiple applications the PSS is used for switching power loads, valves, and pyro devices. Each application has some unique requirements, but in general, they all require power switching. The PSS is comprised of the CIA and four PASMs.

*Power Distribution Function*

The power distribution function uses the PSS to provide load switching, telemetry, and fault protection. The number of slices will depend on the number of loads and total power of the spacecraft.

The command interface is via the standard interface to the spacecraft data bus. The I2C data bus is isolated between the physical and link layers.

The PSS provides the capability to individually command sixteen switches on the board. Switches assigned to loads can be classified as loadshed or non-loadshed. The switches can be commanded in steady state mode or pulse mode. The steady state command turns the load on or off indefinitely. The pulse mode turns ON the switch for a specified duration after a specified delay. Pulse loads can be continued indefinitely with repeated commands.

The switch fault protection is composed of a current limit function and a selectable trip level. With one current limit, other loads on the same power converter are not affected during the isolation of the fault.

Load current telemetry is available for each switch. The analog load current telemetry can be converted to digital telemetry by the command interface. Since telemetry is available on every switch, the power converter efficiencies can be calculated in flight as well as the identification of load variations, drifts and incipient failures.

The PASM can be used in different configurations. Switches can be connected in parallel to reduce the voltage drop for high current loads. It is configurable in series/parallel or bi-directional connection to the load. Additionally, these switches can be configured in various ways to meet critical load requirements or to provide needed cross-strapping between loads.

*Valve Drive Electronics Function*

The PSS is used for the valve drive electronics function, providing the same functionality as in the power distribution function. Timing is more critical, thus, the pulse mode is used for all of the valves.

The PSS provides four cross-strapped outputs to allow a lower valve holding voltage. The lower voltage can be switched from either a central converter or a tap off the battery.

It takes two power switches per valve to hold it in position. One switch is connected directly to the battery to provide the actuation energy. The second switch is connected through a diode to provide the lower voltage holding power.

*Pyro Drive Electronics Function*

The PSS is used for the pyro drive electronics function, providing the same functionality as in the power distribution function. For pyro devices, safety is more critical, thus the enable command and safety inhibit interface is available to provide the additional layers of protection.

The pulse mode is used for all of the pyro commands. The PASM will provide current limiting to ensure load sharing, while simultaneous events occur.

## 6. Expected Results

It is very difficult to compare one generation of power electronics to another. It would be akin to comparing "apples and oranges". Cassini is the closest power system electronics to compare with the X2000 PSE because of the similar functionality.

Cassini used some gate arrays and hybrids while X2000 is using all mixed-signal ASICs and MCMs. The X2000 PSE hardware is configured to perform the functional equivalent of Cassini, ignoring the additional functionality that comes with the new hardware. The following is a table of parameters to compare.

It is clear that the investment in mixed-signal ASICs and MCMs has paid off in an almost two-to-one improvement in mass and volume. However, the impact of maintaining modularity is indicated in the housekeeping power. Each slice requires more power as compared to Cassini.

Using X2000 PSE hardware for a spacecraft as large as Cassini is not an efficient application because of the large number of boards. There is much less packaging efficiency when 33 as opposed to 15 boards are used. As an example, using the same Cassini board size and the X2000 ASICs and MCMs, the functionality could be achieved in only 5 boards rather than 15.

The X2000 PSE is targeted towards much smaller spacecraft than Cassini; however, it is the closest in functionality for the purpose of a benchmark.

## 7. Conclusion

The X2000 PSE development is producing many products beyond the flight hardware deliverables. The purpose of the program is to build a foundation and a process, which subsequent deliveries can leverage and enhance. The building blocks can be used in many other applications outside of the power system. Some of the building blocks could be used to provide motor control electronics or just about any power-switching application.

Table 2: Cassini Comparison

| PARAMETER | EXPLANATION/ CLARIFICATION | Cassini | X2000 PSE |
|---|---|---|---|
| **Recurring Cost** | | $3,420 K | **$3,522 K** |
| **Mass (kg)** | Total Core for Power Distribution | 54.97 Kg | **29.0 Kg** |
| **Power Control Capability** | | 900W | **900W** |
| **Minimum Housekeeping Power** | All switches OFF | **4.80 W** | 7.60 W |
| **Maximum House Keeping Power** | All switches ON | **11.52 W** | 38.00 W |
| **Complexity** | | Medium | **High** |
| **Development Risk** | | Medium | **High** |
| **Operability/Flexibility** | Building blocks need to be useful for all missions, not just 1 | Medium | **High** |
| **Scaleability** | | High | **High** |
| **Grounding/Isolation** | Which implementation gives the optimum grounding | Good | **Good** |
| **Fault containment** | | Small | **medium** |
| **Volume** | | **63,962 cc** | **35,775 cc** |
| **# of Slices** | | 15 | **38** |
| **Shunt Regulator** | Requires 3 PCSs | 1 | **6** |
| **Capacitor Bank** | one board for 1200uF | 0 | **1** |
| **Power Control** | Included in shunt regulator | 1 | **0** |
| **REU** | | 2 | **0** |
| **House Keeping Power** | PCA | 1 | **2** |
| **PD I/O** | | 2 | **0** |
| **Power Distribution (Switches)** | PSS | 6 | **24** |
| **Valve Drive Electronics** | PSS | 0 | **0** |
| **Pyro Drive** | PSS | 2 | **5** |

The flexibility will ultimately improve the overall efficiency of the power system. By having a flexible design which is modular as well as adaptable, power systems on future spacecraft can save time, cost, and mass with a minimum investment of dollars.

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